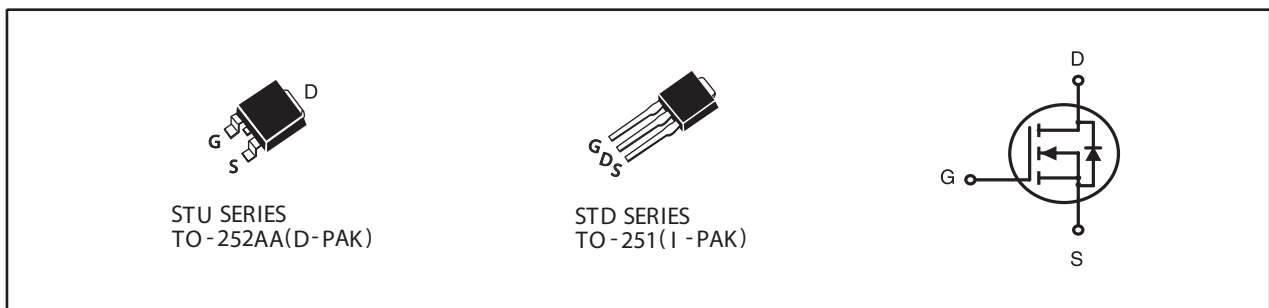


**N-Channel Logic Level Enhancement Mode Field Effect Transistor****PRODUCT SUMMARY**

V <sub>DSS</sub>	I <sub>D</sub>	R <sub>DS(ON)</sub> (mΩ) Typ
100V	35A	20 @ V <sub>GS</sub> =10V

**FEATURES**

- Super high dense cell design for low R<sub>DS(ON)</sub>.
- Rugged and reliable.
- TO-252 and TO-251 Package.

**ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub>=25°C unless otherwise noted)**

Symbol	Parameter	Limit	Units
V <sub>DS</sub>	Drain-Source Voltage	100	V
V <sub>GS</sub>	Gate-Source Voltage	±20	V
I <sub>D</sub>	Drain Current-Continuous <sup>a</sup>	T <sub>C</sub> =25°C	35
		T <sub>C</sub> =70°C	29
I <sub>DM</sub>	-Pulsed <sup>b</sup>	92	A
E <sub>AS</sub>	Single Pulse Avalanche Energy <sup>d</sup>	156	mJ
P <sub>D</sub>	Maximum Power Dissipation <sup>a</sup>	T <sub>C</sub> =25°C	60
		T <sub>C</sub> =70°C	42
T <sub>J</sub> , T <sub>STG</sub>	Operating Junction and Storage Temperature Range	-55 to 175	°C

**THERMAL CHARACTERISTICS**

R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case <sup>a</sup>	2.5	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient <sup>a</sup>	50	°C/W

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## ELECTRICAL CHARACTERISTICS (T<sub>C</sub>=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	V <sub>GS</sub> =0V, I <sub>D</sub> =250uA	100			V
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage <sup>e</sup>	V <sub>GS</sub> =0V, I <sub>D</sub> =10mA	110			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> =80V, V <sub>GS</sub> =0V			1	uA
I <sub>GSS</sub>	Gate-Body Leakage Current	V <sub>GS</sub> = ±20V, V <sub>DS</sub> =0V			±100	nA
<b>ON CHARACTERISTICS</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250uA	2	2.7	4	V
R <sub>DS(ON)</sub>	Drain-Source On-State Resistance	V <sub>GS</sub> =10V, I <sub>D</sub> =17A		20	25	m ohm
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> =10V, I <sub>D</sub> =17A		32		S
<b>DYNAMIC CHARACTERISTICS<sup>c</sup></b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V f=1.0MHz		3160		pF
C <sub>OSS</sub>	Output Capacitance			215		pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			178		pF
<b>SWITCHING CHARACTERISTICS<sup>c</sup></b>						
t <sub>D(ON)</sub>	Turn-On Delay Time	V <sub>DD</sub> =50V I <sub>D</sub> =1A V <sub>GS</sub> =10V R <sub>GEN</sub> = 6 ohm		81		ns
t <sub>r</sub>	Rise Time			85		ns
t <sub>D(OFF)</sub>	Turn-Off Delay Time			115		ns
t <sub>f</sub>	Fall Time			25		ns
Q <sub>g</sub>	Total Gate Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =17A, V <sub>GS</sub> =10V		57		nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>DS</sub> =50V, I <sub>D</sub> =17A, V <sub>GS</sub> =10V		8.5		nC
Q <sub>gd</sub>	Gate-Drain Charge			22		nC
<b>DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS</b>						
V <sub>SD</sub>	Diode Forward Voltage	V <sub>GS</sub> =0V, I <sub>S</sub> =5A		0.77	1.3	V
<b>Notes</b>						
<p>a. Surface Mounted on FR4 Board, t ≤ 10sec.</p> <p>b. Pulse Test: Pulse Width ≤ 300us, Duty Cycle ≤ 2%.</p> <p>c. Guaranteed by design, not subject to production testing.</p> <p>d. Starting T<sub>J</sub>=25°C, L=0.5mH, V<sub>DD</sub> = 50V. (See Figure 13)</p> <p>e. Pulse Test: Pulse Width ≤ 1us, Duty Cycle ≤ 1%.</p>						

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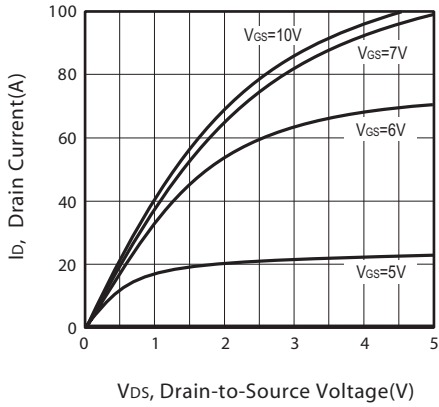


Figure 1. Output Characteristics

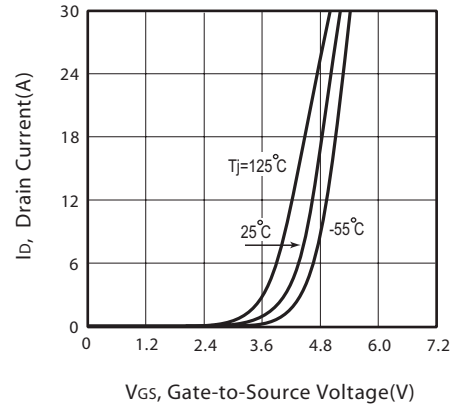


Figure 2. Transfer Characteristics

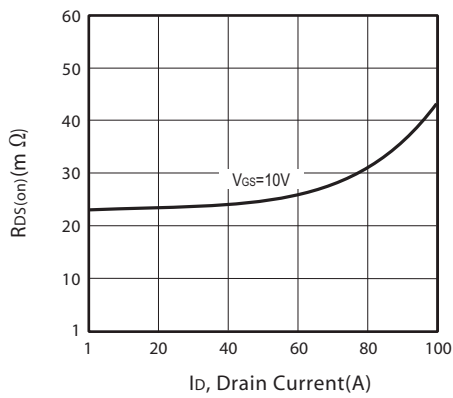


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

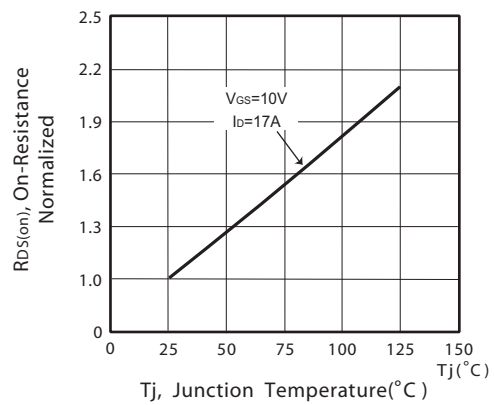


Figure 4. On-Resistance Variation with Drain Current and Temperature

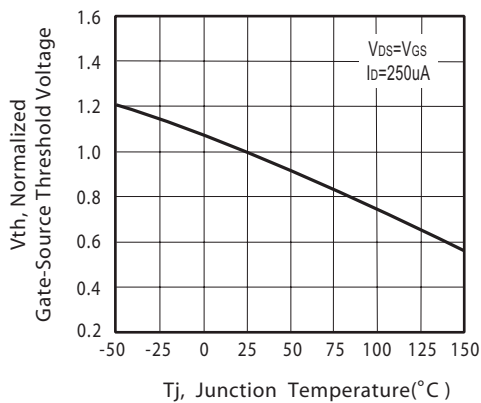


Figure 5. Gate Threshold Variation with Temperature

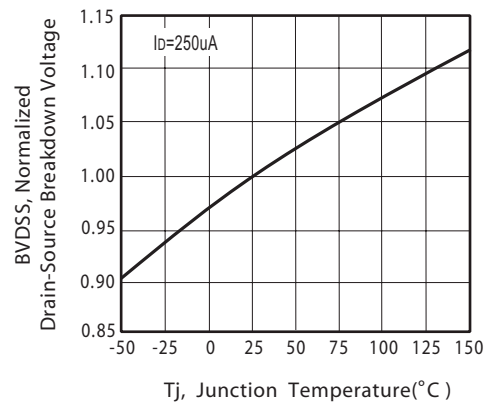


Figure 6. Breakdown Voltage Variation with Temperature

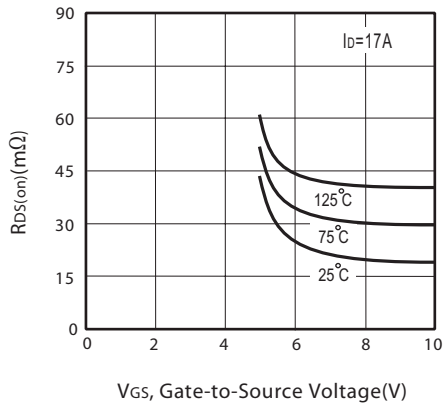


Figure 7. On-Resistance vs. Gate-Source Voltage

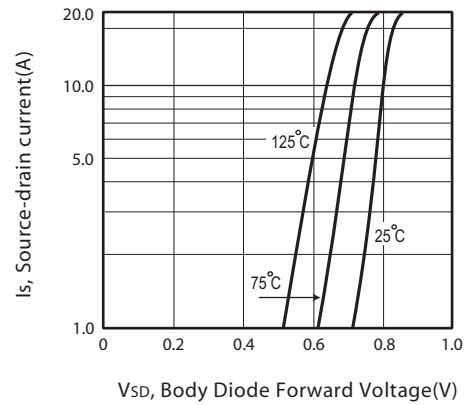


Figure 8. Body Diode Forward Voltage Variation with Source Current

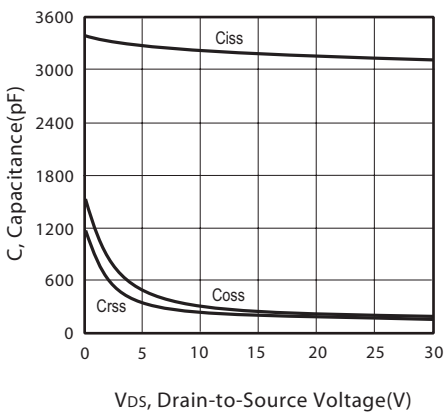


Figure 9. Capacitance

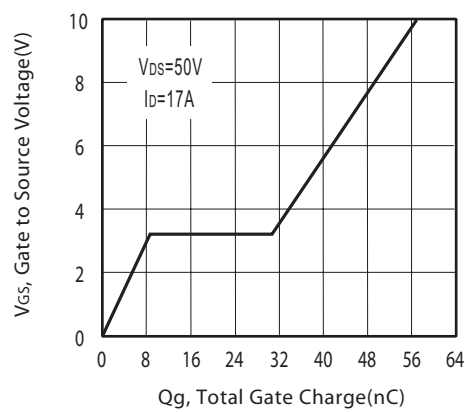


Figure 10. Gate Charge

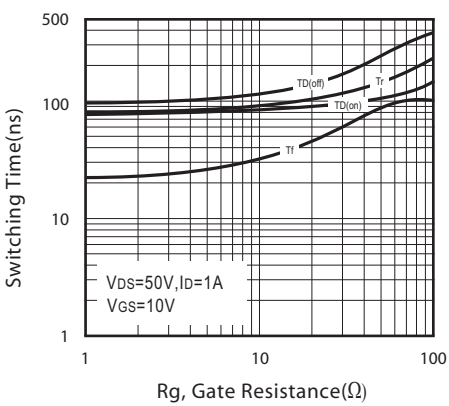


Figure 11. switching characteristics

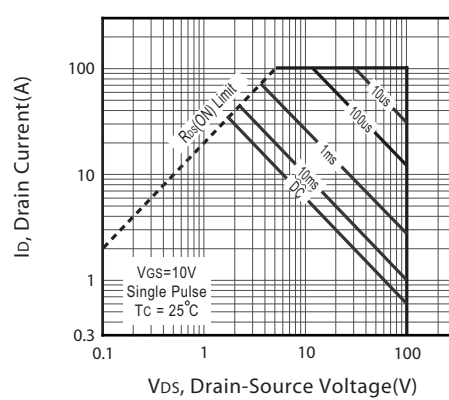
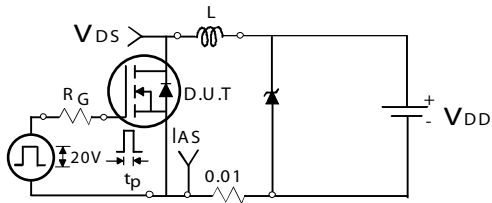
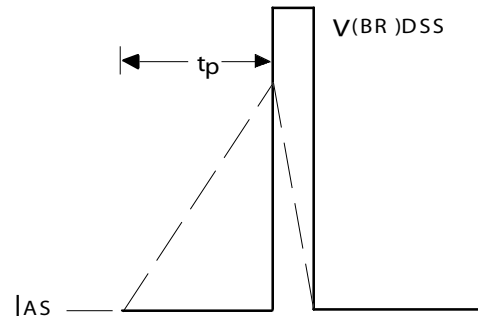


Figure 12. Maximum Safe Operating Area



Unclamped Inductive Test Circuit

Figure 13a.



Unclamped Inductive Waveforms

Figure 13b.

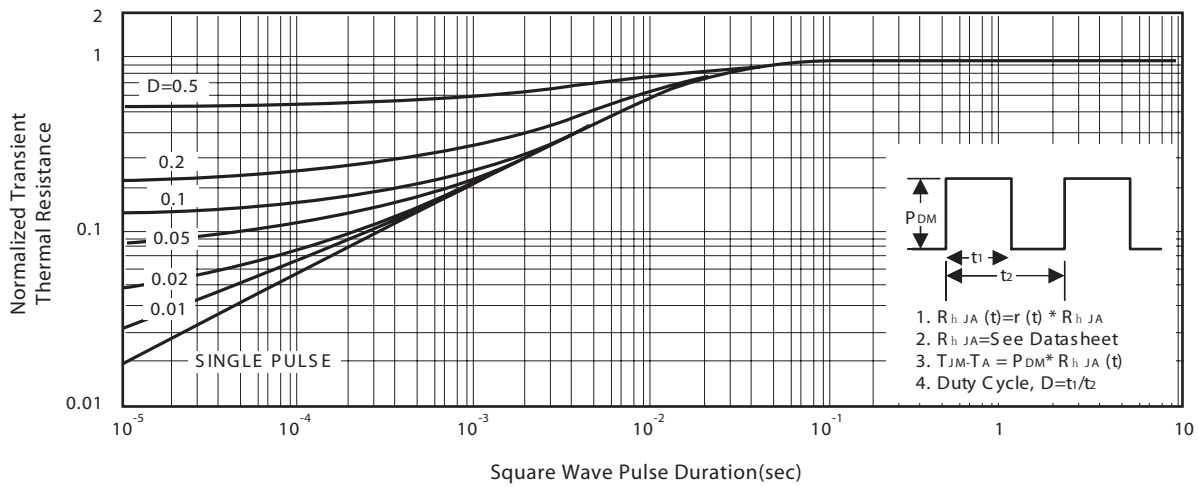
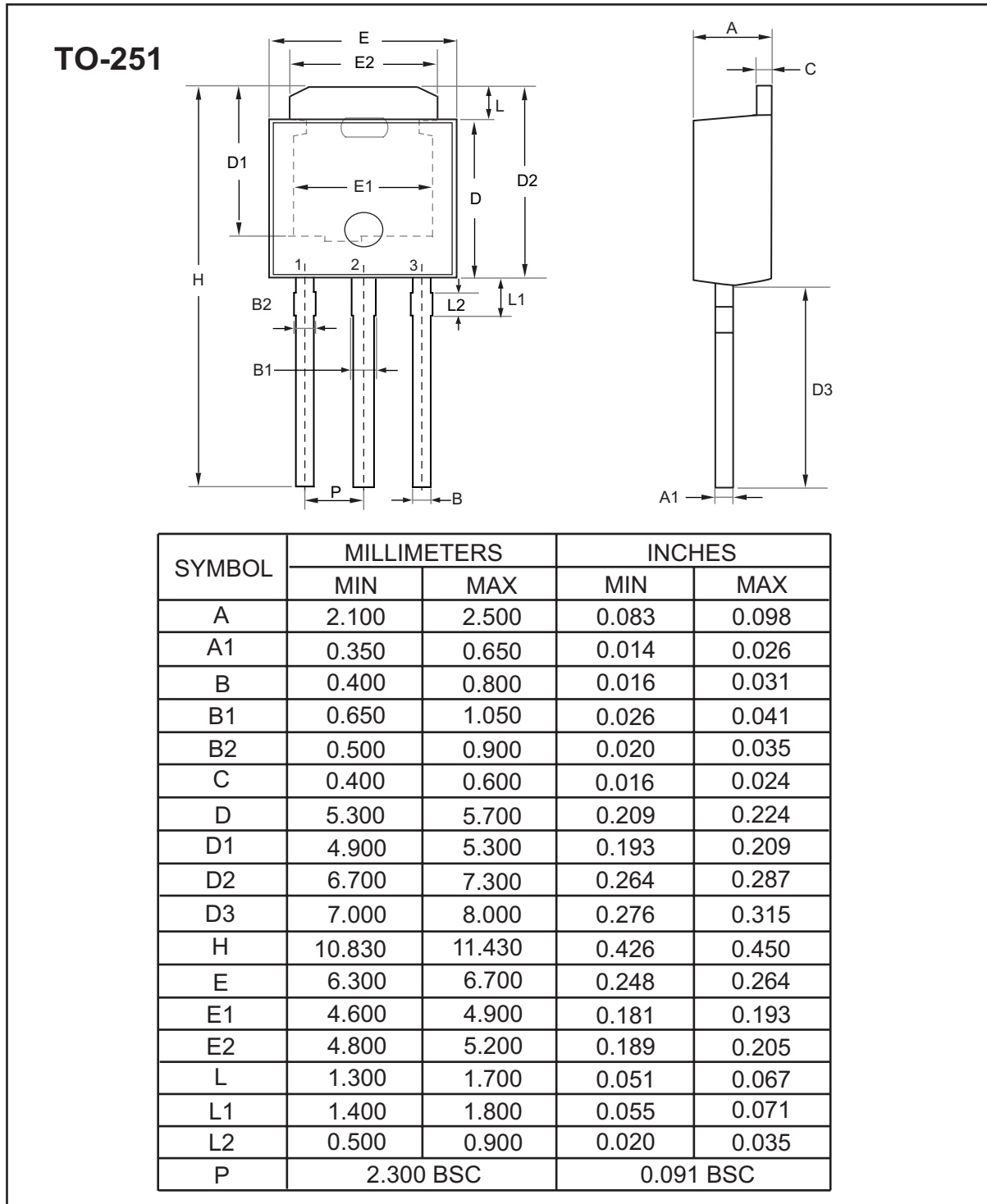


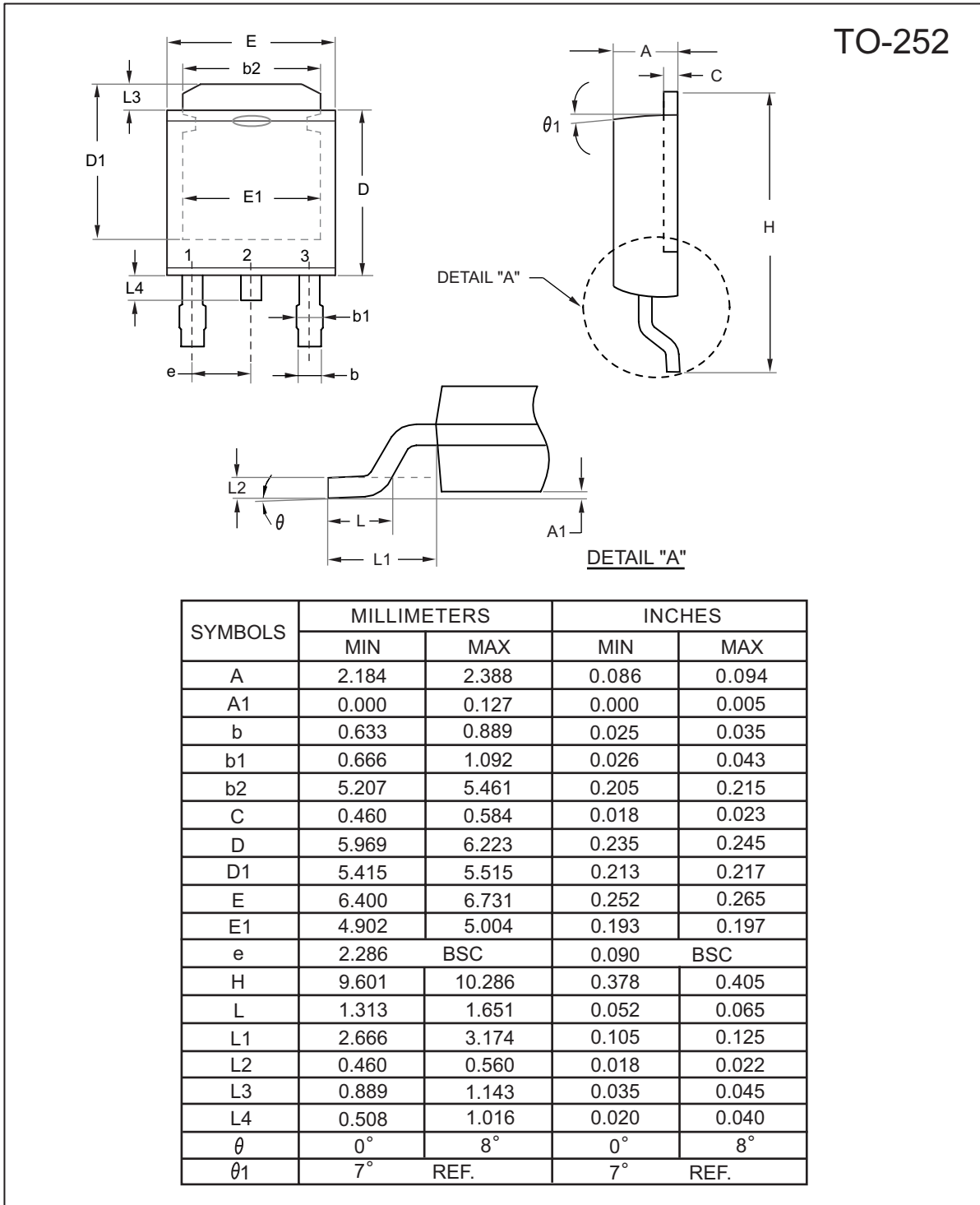
Figure 14. Normalized Thermal Transient Impedance Curve

## PACKAGE OUTLINE DIMENSIONS



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## TO-251 Tube/TO-252 Tape and Reel Data

### TO-251 Tube



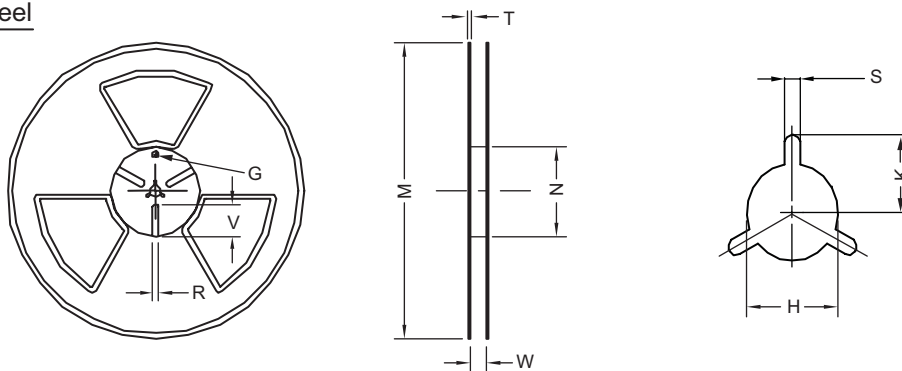
### TO-252 Carrier Tape



UNIT:mm

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
TO-252 (16 mm)	6.96 ±0.1	10.49 ±0.1	2.79 ±0.1	φ 2	φ 1.5 + 0.1 - 0	16.0 ±0.3	1.75 ±0.1	7.5 ±0.15	8.0 ±0.1	4.0 ±0.1	2.0 ±0.15	0.3 ±0.05

### TO-252 Reel



UNIT:mm

TAPE SIZE	REEL SIZE	M	N	W	T	H	K	S	G	R	V
16 mm	φ 330	φ 330 ± 0.5	φ 97 ± 1.0	17.0 + 1.5 - 0	2.2	φ 13.0 + 0.5 - 0.2	10.6	2.0 ±0.5	---	---	---